Clock Gating and Precomputation Based Low Power ALU Design
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Abstract — Power reduction in dynamic circuits became an important factor today. In this thesis, we designs an ALU using the popular power reduction techniques named clock gating and precomputation based sequential logic optimization for low power. It reduces the power consumption by reducing the dynamic switching power.

Power reduction deals with synthesis, design at circuit level and placement and routing stages, now moved to the System Level and Register Transfer Level. This is possible due to clock gating which always switch off the inactive unit of the design and reduce overall power consumption. The Register Transfer Level approach is always important because hardware designers generally verify power only at the gate level and any changes to the Register Transfer Level needs many design repetition to reduce power. Our designed ALU has 16 functions. Each functions will carries separate modules. This is because we need not to more than one operation at a time. When we use to operate one functional module, the other modules are not in use by the current executing instruction. At that time we will power off the other 15 modules by using the clock gating technique. Thereby we can reduce the switching power of the other unused modules.

In the proposed system, we further modifies the clock gated ALU with another power consumption method of precomputation based low power architecture. The simulation is done by using Xilinx ISE 13.2 and we implement the design by using FPGA.

Keywords- ALU, Clock Gating, Dynamic power, FPGA, precomputation, RTL.

1 INTRODUCTION

Today, with the advent of the consumer era and the popularity of mobile applications, power optimization became the mantra of the day. Designers go through several iterations to optimize power in order to achieve their power budgets. Though power should be optimized at all stages of the design flow, optimizations in early design stages have the greatest impact in reducing power.

In this thesis, designing an ALU with reduced dynamic power. For the dynamic power reduction, here using two important methods of, clock gating technique and precomputation based sequential logic optimization.

2 LITERATURE REVIEW

Clock power consumes 50-70 percent of total chip power and is expected to significantly increase in the next generation of designs at 45nm and below [1]. This is due to the fact that power is directly proportional to voltage and the frequency of the clock as shown in the following equation:

\[ \text{Power} = \text{Capacitance} \times (\text{Voltage})^2 \times (\text{Frequency}) \]

Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by many designers and is typically implemented by gate-level power synthesis tools.

A. Clock gating principle

Clock gating, which is one of the most well-known low-power techniques, is very effective in reducing the power consumption in digital circuits and also VLSI circuits. The goal of this technique is to disable or suppress transitions from propagating to parts of the clock path (i.e., flip-flops, clock network, and logic) under a certain condition computed by clock-gating circuits. The savings are mainly due to the switching capacitance reduction in the clock network and the switching activity in the logic fed by the storage elements because unnecessary transitions are not loaded when the clock is not active.

The CG is illustrated in figure 1, block CG, which inhibits the clock signal when the idle condition is true, is associated with each sequential functional unit. The clock signal is computed by function Fcg. CLK is the system clock and CLKG the gated clock of the functional unit.
B. Clock gating styles

There are many clock gating styles available to optimize power in VLSI circuits. They can be:
1) Latch-free based design.
2) Latch-based design.
3) Flip-flop based design.
4) Intelligent clock gating optimizing option available in synthesis tool like Xilinx, Altera, Cadence SOC Encounter etc.

This paper presents the experiments of power consumption using different techniques to turn off part of a system and switch between active and standby modes. The main ideas analyzed here are: clock gating, clock enable and blocking inputs [1]. The laboratory work is described, including the measurement setups and the benchmark circuits. The selected circuits used as benchmarks are different type of multipliers. The results of power consumption in active and standby modes are presented and compared. The first point is that turning off that part of the system in any of the three techniques always Improves the power figure. The best option is to use global clock gating. The use of clock enable is good option when the design does not have large amount of flip flops.

The work in the paper investigates the various clock gating techniques that can be used to optimize power in VLSI circuits at RTL level and various issues involved while applying this power optimization techniques at RTL level. Power optimization, traditionally relegated to the synthesis, and placement and routing stages, has moved up to the System level and RTL stages. Hardware designers use clock gating to turn off inactive sections of the design and reduce overall dynamic power consumption.

RTL Clock Gating is the most commonly used optimization technique for reducing dynamic power [4]. The challenge of optimizing power by adding clock gating is knowing where and when to insert clock gating. The traditional method of looking at the percentage of registers that are clock gated is not indicative of the power savings because it does not take into account switching activity. The average Clock-Gating Efficiency for a design is a much better indicator of dynamic power consumption because it is a measure of both how many and how long registers are gated.

The paper [5] has revisited the well-known clock gating technique to analyse the abilities of different CG styles to save both dynamic and leakage power at a FF level, depending on the input activity. Useful optimization procedures and guidelines are presented for leakage reduction. Focusing on those structures that do not need a latch to remove undesired transitions in gated clock, a leakage reduction of a fourth of the original one is achieved without degradation in timing performances. Although a positive-edge-triggered FF was used as reference, the results are immediately extended to a negative-edge triggered FF, but using those CG styles that set clk to low.

The reference [3] presents the design and implementation of a Self-Timed Arithmetic Logic Unit that has been developed as part of an asynchronous microprocessor. This displays an inherent operational characteristic of low consumption, owing to the synchronization signals that stop when the execution of an operation finishes (stopable clock); that is to say, the dynamic consumption is zero, while it is not required again by an external request signal. It demonstrates the methodology of design of the Self-Timed controls which synchronize the data transfer, as well as the characterization of delay macros designed in FPGA editor for the adjustment of ALU processing times.

A low power 16-bit ALU has been designed, fabricated and tested at the transistor level. The designed ALU performs 16 instructions and has a two-stage pipelined architecture. For low power consumption, we propose a new ALU architecture which has an efficient ELM adder of propagation (P) and generation (G) block scheme [3]. The operation of an adder of the proposed ALU is disabled while the logical operation is performed and vice versa, and outputs of P block are separated to become dual bus to reduce switching capacitances during the ALU operation. Double edge-triggered pip-flops are used to reduce the switching activity for the register.
C. Functional description of ALU

The proposed ALU is a 16 bit ALU that performs 16 functions. Each separate function is provided 16 separate select bits. The select bits start from 0000 upto 1111. For selecting any one of the operation, the multiplexer will receives the appropriate ALU function.

D. Precomputation technique

This method deals with the problem of reducing the power by optimizing logic-level sequential circuits. Alidina proposed a powerful sequential logic optimization method to reduce power that is based on selectively precomputing the output logic values of the circuit one clock cycle before they are required, and using the precomputed values to reduce internal switching activity in the succeeding clock cycle[9]. The main objective of this technique is to synthesize the precomputation logic, which predicts the output of a subset of inputs for the next value. The original logic circuit can be switched off in the next clock cycle by using a latch if the outputs can be precomputed using the precomputation logic. The precomputation logic takes as its inputs the current inputs of the circuit and computes the output value. The important factor in this method is that the power savings that are achieved by implementing this technique should overcome the power that is dissipated by the additional circuitry that is
added for the precomputation logic to select the inputs for which the output is precomputed.

![Precomputation Architecture](image)

Fig. 4 precomputation architecture

In CMOS circuits the probabilistic average switching activity of a circuit is a good measure of average power dissipation of the circuit. Average power dissipation can be thus computed by estimation the average switching activity.

3 SIMULATION AND IMPLEMENTATION

Xilinx ISE Design Suite 12.3 platform is used for the simulation and synthesis of this proposed architecture. The hardware description language verilog HDL is used for implementation of the proposed architecture. Spartan 3E FPGA is used for the implementation of the precomputation-based ALU architecture after the simulation and synthesis in Xilinx ISE Design Suite 13.2.

4 RESULT

PERFORMANCE ANALYSIS

The main advantage of this thesis is to reduce the dynamic power. For that here we using two techniques.

1. Clock gating
2. Precomputation based power reduction

<table>
<thead>
<tr>
<th>Method</th>
<th>total power(w)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip flop based CG - ALU</td>
<td>0.052</td>
</tr>
<tr>
<td>Precomputation based ALU</td>
<td>0.014</td>
</tr>
</tbody>
</table>

Table 2 Power Comparison

![Power Comparison Graph](image)

Fig. 5 Dynamic Power (nW) Comparison of CG Cells

5 CONCLUSION

Power reduction deals with synthesis, design at circuit level and placement and routing stages. In this paper we moved to the System Level and Register Transfer Level. This is possible due to clock gating which always switch off the inactive unit of the design and thus reduce overall power consumption. Our designed ALU has 16 functions. Each function has one dedicated module. When one instruction executes in their respective module, others module that was not used by current executing instruction must gated off by the clock gate. Here, further power consumption is possible by the modification which is, the introduction of Precomputation-based sequential logic optimization for low power.

Here, when using clock gating technique, when any one of module execute because of clock gating, rest 15 modules turned off and hence reduce power upto 93.75%.

\[
\text{Power Reduction} = \frac{15}{16} \times 100 = 93.75\%
\]

The modification of this paper is the method to reduce power that is based on selectively precomputing the output logic values of the circuit one clock cycle before they are required, and using the precomputed values to reduce internal switching activity in the succeeding clock cycle. Many low power design techniques have been developed nowadays. And most of them can be applied simultaneously. A new logic level low power synthesis is presented here in this project. The main target is to reduce the switching activities. The performance like reduction in switching activity, area and critical path delay of this method is better than previous methods.
6 FUTURE SCOPE

Clock gating technique is one of the best techniques to reduce dynamic power. There is need to extend clock gating technique to reduce leakage power consumption. Virtex-6 FPGA is based on 40-nm technology. Latest FPGA like Virtex-7, Kintex-7, Artex-7 based on 28-nm technology contribute significant leakage power consumption. There is need to optimize clock gating to reduce leakage power along with dynamic power.

Accurate power estimation is possible by using this precomputation based technique. The extension of this method to data path components should be useful for pipelined ALU. The remitting circuit will optimize the power and speed also. The testability of issues also high.

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REFERENCES


